

NEW

PATENT

AMENDMENT A (PRELIMINARY)

SPECIFICATION AMENDMENTS

At page 1, lines 1-2, please amend the Title as follows:

~~MICROPROCESSOR WITH HARDWARE CONTROLLED POWER~~
~~MANAGEMENT SIGNAL-INITIATED METHOD FOR SUSPENDING~~
~~OPERATION OF A PIPELINED DATA PROCESSOR~~

At page 1, between lines 2 and 3, please insert the following:

RELATED APPLICATIONS

This is a division of U.S. patent application no. 10/216,615, filed August 9, 2002.

At page 1, lines 4-6, please amend the text of the section entitled "Technical Field of the Invention" as follows:

This invention relates in general to integrated circuits, and more particularly to a ~~microprocessor having hardware controlled pipelined data processor with power management control~~.

At page 4, lines 3-21, please amend the text of the section entitled "Summary of the Invention" as follows:

~~—In accordance with the present invention, a method and apparatus is provided which provides significant advantages in reducing the power consumption of a microprocessor.~~

~~—In the present invention, a processing unit includes a plurality of subcircuits and circuitry for generating a clock signal thereto. Circuitry is provided for detecting the assertion of a control signal; responsive to the control signal, disabling circuitry disables the clock signal to one or more of the subcircuits.~~

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~~_____The present invention provides significant advantages over the prior art. A significant reduction in the power consumed by a computer may be effected by disabling the clock to the microprocessor circuitry. The present invention allows the disabling and enabling of the microprocessor clock signals to be controlled by a single control signal. Further, an acknowledge signal may be provided to notify external circuitry of the suspended state of the microprocessor.~~

_____In accordance with the presently claimed invention, a signal-initiated method for suspending operation of a pipelined data processor is provided by selectively disabling a clock signal to pipeline subcircuitry in response to at least one control signal.

_____In accordance with one embodiment of the presently claimed invention, a method for suspending operation of a pipelined data processor to reduce power consumption includes:

_____enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

_____advancing a sequence of instructions to a first portion of a pipeline subcircuit;

_____executing the advanced sequence of instructions with a second portion of the pipeline subcircuit subsequent to the first pipeline subcircuit portion in response to the enabled first clock signal; and

_____detecting an occurrence of a second combination of the respective states of the one or more clock control signals and in response thereto

_____interrupting the advancing of the sequence of instructions to the first pipeline subcircuit portion, followed by

_____executing with the second pipeline subcircuit portion a plurality of microcode substantially unrelated to the sequence of instructions in response to the enabled first clock signal, and followed further by

_____disabling the first clock signal.

_____In accordance with another embodiment of the presently claimed invention, a method for suspending operation of a pipelined data processor to reduce power

consumption includes:

_____ enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

_____ advancing a sequence of instructions to a first portion of a pipeline subcircuit;

_____ executing the advanced sequence of instructions with a second portion of the pipeline subcircuit subsequent to the first pipeline subcircuit portion in response to the enabled first clock signal; and

_____ detecting an occurrence of a second combination of the respective states of the one or more clock control signals and in response thereto

_____ interrupting the advancing of the sequence of instructions to the first pipeline subcircuit portion, followed by

_____ generating a plurality of address data and

_____ executing with the second pipeline subcircuit portion a plurality of microcode corresponding to the plurality of address data and substantially unrelated to the sequence of instructions in response to the enabled first clock signal, and followed further by

_____ disabling the first clock signal.

_____ In accordance with another embodiment of the presently claimed invention, a method for suspending operation of a pipelined data processor to reduce power consumption includes:

_____ enabling a first clock signal in response to an occurrence of a first combination of respective states of one or more clock control signals;

_____ advancing a sequence of instructions to a first portion of a pipeline subcircuit;

_____ executing the advanced sequence of instructions with a second portion of the pipeline subcircuit subsequent to the first pipeline subcircuit portion in response to the enabled first clock signal; and

_____ detecting an occurrence of a second combination of the respective states of the one or more clock control signals and in response thereto

_____ interrupting the advancing of the sequence of instructions to the first

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pipeline subcircuit portion, followed by
_____ generating a plurality of address data,
_____ addressing the first pipeline subcircuit portion with the plurality of
address data and in response thereto generating a plurality of microcode substantially
unrelated to the sequence of instructions, and
_____ executing the plurality of microcode with the second pipeline
subcircuit portion in response to the enabled first clock signal, and followed further by
_____ disabling the first clock signal.

At page 19, lines 3-8, please amend the text of the section entitled “Abstract of the Disclosure” as follows:

~~A processing unit includes a plurality of subcircuits and circuitry for generating clock signals thereto. Detection circuitry detects the assertion of a control signal and disabling circuitry is operable to disable the clock signals to one or more of the subcircuits responsive to the control signal.~~ A signal-initiated method for suspending operation of a pipelined data processor by selectively disabling a clock signal to pipeline subcircuitry in response to at least one control signal.